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Ann Gordon-Ross, Susan Cotterell, Frank Vahid
November 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 4
Full text available: 🔲 pdf(887.71 KB)   Additional Information: full citation, abstract, references, index terms

Instruction caches have traditionally been used to improve software performance. Recently, several tiny instruction cache designs, including filter caches and dynamic loop caches, have been proposed to instead reduce software power. We propose several new tiny instruction cache designs, including preloaded loop caches, and one-level and two-level hybrid dynamic/preloaded loop caches. We evaluate the existing and proposed designs on embedded system software benchmarks from both the Powerstone and ...

Keywords: Loop cache, architecture tuning, embedded systems., filter cache, fixed program, instruction cache, low energy, low power

2 Efficient management of memory hierarchies in embedded DRAM systems
Ashley Saulsbury, Su-Jaen Huang, Fredrik Dahlgren
May 1999 **Proceedings of the 13th international conference on Supercomputing**
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Keywords: COMA, DRAM, cache, latency, memory hierarchy, processor

3 Memory optimization for embedded systems: Improved indexing for cache miss reduction in embedded systems
Tony Givargis
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: 🔲 pdf(215.59 KB)   Additional Information: full citation, abstract, references, index terms

The increasing use of microprocessor cores in embedded systems as well as mobile and portable devices creates an opportunity for customizing the cache subsystem for improved performance. In traditional cache design, the index portion of the memory address bus consists of the K least significant bits, where K=log2(D) and D is the depth of the cache. However, in devices where the application set is known and characterized (e.g., systems that execute a fixed application set) there is an opportunity ...

Keywords: cache optimization, design space exploration, index hashing

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2 **On the use of trace sampling for architectural studies of desktop applications**
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3 **Expected I-cache miss rates via the gap model**
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